LISTING OF THE CLAIMS:

1. (Original) A programmable read-only memory cell, comprising:

a source electrode;

a drain electrode;

a channel layer formed between the source electrode and the drain electrode;

a floating gate isolated from the channel layer; and

a selection gate isolated from the channel layer, wherein the selection gate and the floating gate are arranged on opposite sides of the channel layer, and wherein a first insulator layer is arranged between the floating gate and the channel layer and a second insulator layer is arranged between the selection gate and the channel layer.

2. (Original) The programmable read-only memory cell of claim 1, wherein the floating gate is arranged at least partly in a trench of a substrate, wherein the trench is formed between the source electrode and the drain electrode, and wherein the floating gate is electrically insulated from the substrate.

3. (Original) The programmable read-only memory cell of claim 2, wherein the floating gate is insulated from the substrate by a thin insulator layer formed as an oxide-nitride-oxide layer.

4. (Original) The programmable read-only memory cell of claim 2, wherein a trench capacitor is formed in the substrate, an inner electrode of said trench capacitor being formed by the floating gate and an outer electrode of said capacitor being formed by a first diffusion region.

5. (Original) The programmable read-only memory cell of claim 4, wherein the first diffusion region is formed within a second diffusion region and the second diffusion region is formed within a third diffusion region, the second diffusion region having a complementary doping with respect to the first diffusion region and with respect to the third diffusion region.

6. (Original) The programmable read-only memory cell of claim 4, wherein the first diffusion region of the read-only memory cell has an overlap region with one or more first diffusion regions of two read-only memory cells of a matrix-type arrangement of read-only memory cells that are directly adjacent in a direction perpendicular to a word line, and wherein the overlap region forms an electrically conductive connection between the first diffusion regions of a plurality of read-only memory cells in a series.

7. (Original) The programmable read-only memory cell of claim 1, wherein the channel layer is formed as an epitaxial layer.

8. (Original) The programmable read-only memory cell of claim 1, wherein the channel layer has an n-type doping.

9. (Original) The programmable read-only memory cell of claims 1, wherein the source electrode and the drain electrode are formed at least partly on a surface of a substrate.

10. (Original) A method for operating a programmable read-only memory cell, comprising:

writing to the programmable read-only memory cell by applying an activating electrical voltage between a selection gate and one of a source electrode and a drain electrode to open a channel in a channel layer formed between the source electrode and the drain electrode, and applying a programming electrical voltage between a first diffusion region and the channel layer, wherein one of the source electrode and the drain electrode is put at a negative programming electrical potential, the first diffusion region is put at a positive programming electrical potential and the selection gate is put at an activating positive electrical potential.

11. (Original) The method of claim 10, further comprising:

erasing an information item of the programmable read-only memory cell by applying the activating electrical voltage between the selection gate and one of the source electrode and the drain electrode to open the channel and applying an erasing electrical voltage between the first diffusion region and the channel layer, wherein one of the source electrode and the drain electrode is put at a positive erasing electrical potential, the first diffusion region is put at a negative erasing electrical potential and the selection gate is put at an activating positive electrical potential.

12. (Original) The method of claim 11, further comprising:

reading out the information item of the programmable read-only memory cell by applying a reading electrical voltage between the source electrode and the drain electrode, wherein the source electrode is put at ground potential, wherein the drain electrode, the selection gate and the first diffusion region are put at a positive reading electrical potential and determining a conductivity of the channel layer, said conductivity depending on the charge state of the read-only memory cell.

13. (Original) A programmable read-only memory cell, comprising:

a floating gate disposed in a trench of a substrate;

a channel layer formed over the floating gate, connecting a source electrode to a drain electrode; and

a selection gate disposed above the channel layer.

14. (Original) The programmable read-only memory cell of claim 13, further comprising:

a first insulator layer disposed between the floating gate and the channel layer; and

a second insulator layer disposed between the selection gate and the channel layer.

15. (Original) The programmable read-only memory cell of claim 14, further comprising:

an insulator layer disposed between the floating gate and the substrate.

16. (Original) The programmable read-only memory cell of claim 15, further comprising:

a trench capacitor, formed in the substrate, comprising an inner electrode formed by the floating gate and an outer electrode formed by a first diffusion region disposed between the insulator layer and the substrate.

17. (Original) The programmable read-only memory cell of claim 16, further comprising:

a second diffusion region surrounding the first diffusion region; and

a third diffusion region surrounding the second diffusion region, wherein the second diffusion region has a complementary doping with respect to the first diffusion region and with respect to the third diffusion region.

18. (Original) The programmable read-only memory cell of claim 17, wherein the first diffusion region has one or more overlap regions with one or more adjacent first diffusion regions of adjacent read-only memory cells in a direction perpendicular to a word line, and wherein the one or more overlap regions form an electrically conductive connection between adjacent first diffusion regions.

19. (Original) The programmable read-only memory cell of claim 17, wherein the channel layer is formed as an epitaxial layer having an n-type doping, and wherein the channel layer is isolated from the floating gate and the selection gate.

20. (Original) The programmable read-only memory cell of claim 17, wherein the source electrode and the drain electrode are formed at least partly on a surface of a substrate.